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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,169	09/12/2003	Norman W. Robson	FIS920030257US1	2168

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,169	ROBSON ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/605169 filed on 09/12/2003, claims 1-20 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 and 17 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Applicant has stated, "testing at least one parameter of said subset of transistors", this statement is failed to mention any parameter in a subset transistor to set forth the subject matter before performing the test.

4. Claims 1, 17 and 20 recites the limitation "semiconductor material". There is insufficient antecedent basis for this limitation in the claim.

5. Claims 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has stated, " modifying a step in said integrated circuit process", but the specification has not mention any step of modification and which step in integrated circuit process is going to be modified.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1- 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Voogel (US 6,281,696) in view of Leedy (US 5,654,127).

8. **With respective to claim 1, 17, and 20** Voogel discloses a method of testing an integrated circuit structure comprising the steps of:

(as claim 1, 17, and 20) providing a semiconductor wafer containing a set of chip locations for forming a set of integrated circuits therein (fig. 2A; col. 4 ll. 64-67 and col. 5, ll. 1-9 – wafer 200, each location (IC region 140) include one or more transistor of IC 110, 300, which are provided multiple testing circuit--);

(as claim 1, 17, and 20) fabricating in said wafer a set of transistors specific to a particular integrated circuit in said chip locations (col. 1, ll. 30-35 and ll. 44-47 – fabricate a layout of basic cell, example transistors on the silicon wafer-- and fig. 3A – 3D; col. 6, ll. 47-61 – fabricate IC 110 in location (IC region 140) on wafer 200 in figure 2A and 2B--);

(as claim 1, 17, and 20) connecting at least one subset of transistors by a lithographic process in at least one chip location (col. 1, ll. 30-33 and ll. 47-51 – a layout consists of set of patterns, which are correspond to formation of transistor and interconnect structure, these patterns will be transferred on to silicon wafer using photolithographic (lithographic) (photolithographic – the most common lithography technique in semiconductor manufacturing--) and film formation process --) in a test interconnect arrangement using interconnect levels close to said semiconductor

material (col. 6, ll. 47-67 and col. 10, ll. 15-20 – the wafer is tested only up to metal 2 --); and

(as claim 17) testing at least one parameter (voltage and current) of said subset of transistors (col.9, ll. 19-23, ll. 4043, and ll. 55-60 – testing or detecting a open and short circuit based on voltage source and current output--).

Voogel does not teach the modification step in the integrated circuit process.

Leedy teaches the rip-up router software, which is a tool to make local change by modified netlist in next used to produce the database for desired interconnect pattern on the wafer using E-beam lithographic (col. 6, ll. 33-51) when the data resulting from tester signal processor is list of the location of each defective transistor (col.5, ll.26-28).

It would have been obvious at the time of invention was made to one of ordinary skill in the art would combine references Voogel and Leedy of using an automatic router rip-up tool interface with E-bean lithographic for routing (connecting) a subset transistors (Voogel, col. 1, ll. 30-33 and ll. 47-51; Leedy, col. 3, ll. 15-20) and also modifying the netlist of interconnection database in the next used, if any defective transistor occurred during the fabrication process (Leedy, col.5, ll. 47-60). Moreover, the rip-up router provides a flexibility in changing the existing IC metallization layout, accepting a new command of placement netlist and computing of changing IC metallization in database with less cost and more efficiency, and the rip-up router is also the standard software used to drive the E-beam lithography equipment (Leedy, col. 6, ll. 15-50).

9. **With respective to claim 2,** all the limitations as set forth claims rejected above, further discloses the test arrangement is constructed using only a first interconnect level above said set of transistors (Voogel, col. 3, ll. 34-38; Leedy, col. 16, ll. 1-10 and col. 6, ll. 42-57 – after fabricating a first metal (interconnect) layer, then performing a test --).

10. **With respective to claim 3,** all the limitations as set forth claims rejected above, further discloses the test arrangement is constructed using both a first and second interconnect level above said set of transistors (Voogel, col. 10, ll. 18-20; Leedy, col. 16, ll. 1-10 and col. 6, ll. 42-57 – after fabricating a first metal (interconnect) layer, then performing a test, and then repeat for second metal (interconnect) layer--).

11. **With respective to claims 4-7,** all the limitations as set forth claims rejected above, further discloses the subset comprises at least two sub-circuits module of said integrated circuit (Voogel, col. 1, ll. 20-27; Leedy, col. 17, ll. 18-22).

12. **With respective to claim 8,** all the limitations as set forth claims rejected above, further discloses test comprises providing an input test vector and recording output signals from said test structure (Voogel, col. 1, ll. 27-30 and ll. 44-47; Leedy, col. 20. ll. 21-28 and col. 5, ll. 26-35).

13. **With respective to claim 9,** all the limitations as set forth claims rejected above, further discloses a step of removing said test interconnect arrangement and depositing layer of said integrated circuit an interconnect in replacement thereof (Leedy, col. 6, ll. 42-57).

14. **With respective to claim 10,** all the limitations as set forth claims rejected above, further discloses the test arrangement is constructed using only a first

interconnect level above said set of transistors (Voogel, col. 3, ll. 34-38; Leedy, col. 16, ll. 1-10 and col. 6, ll. 42-57 – after fabricating a first metal (interconnect) layer, then performing a test --).

15. **With respective to claim 11,** all the limitations as set forth claims rejected above, further discloses the test arrangement is constructed using both a first and second interconnect level above said set of transistors (Voogel, col. 10, ll. 18-20; Leedy, col. 16, ll. 1-10 and col. 6, ll. 42-57 – after fabricating a first metal (interconnect) layer, then performing a test, and then repeat for second metal (interconnect) layer--).

16. **With respective to claims 12-15,** all the limitations as set forth claims rejected above, further discloses the subset comprises at least two sub-circuits module of said integrated circuit (Voogel, col. 1, ll. 20-27; Leedy, col. 17, ll. 18-22).

17. **With respective to claim 16,** all the limitations as set forth claims rejected above, further discloses test comprises providing an input test vector and recording output signals from said test structure (Voogel, col. 1, ll. 27-30 and ll. 44-47; Leedy, col. 20. ll. 21-28 and col. 5, ll. 26-35).

18. **With respective to claim 18,** all the limitations as set forth claims rejected above, further discloses the test arrangement is constructed using only a first interconnect level above said set of transistors (Voogel, col. 3, ll. 34-38; Leedy, col. 16, ll. 1-10).

19. **With respective to claims 19,** all the limitations as set forth claims rejected above, further discloses the test arrangement is constructed using both a first and

second interconnect level above said set of transistors (Voogel, col. 10, ll. 18-20; Leedy, col. 16, ll. 1-10).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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09/04/2005